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EXAMINER

WILLIAMS, HOWARD L

ART UNIT PAPER NUMBER

2819

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/821,487
Filing Date: April 09, 2004
Appellant(s): REZEQ ET AL.

MAILED
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GROUP 2800

Alan K. Stewart
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 17 February 2006 appealing from the Office action mailed 20 September 2005.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

No amendment after final has been filed, throughout this prosecution only arguments have been filed in the responses.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5079551	Kimura et al.	1-1992
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(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

35 U.S.C. 102(b):

*A person shall be entitled to a patent unless –
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.*

Claims 1-28 are rejected under 35 U.S.C. 102(b) as anticipated by U.S. Patent 5079551 to Kimura et al. Kimura et al. discloses an accumulator system for a delta-sigma modulator with the bits grouped by significance to a lower order group and higher order group. The carry bits from each accumulator stage are separately determined and passed up to the corresponding stage. Pre-accumulator logic for the higher order

accumulator chain is embodied in delay element 32; fig. 1. with various inter-accumulator delay embodied by delay elements 36, 38, 42, 46, 48 and 52; all in fig. 1. Applicant claims an additional accumulator chain in claims 6, 14 and 24; Kimura although illustrating two chains in the figures also discloses in column 6, lines 42-43 that the principles are applicable to tertiary or higher order $\Sigma\Delta$ modulators also.

It also notable that the description filed provides that the splitter, accumulators, and combiner employed in the disclosed circuit are described as conventional pages 9, 10, 13, 14 and 19.

(10) Response to Argument

Appellants' argument appears limited to that which appears on page 7 of the brief:

That the references of record do not show, teach or suggest these limitations, the Kimura reference does not show, teach or suggest the accumulator chains of claim 1, that US Patent 5,079,551 (i.e. Kimura et al.) discloses an addition circuit for adding feedback digital data to input data, and that U.S. Patent 5,079,551 (i.e. Kimura et al.) does not show accumulator chains.

The brief appears to copy the remarks presented in the responses filed 11 August 2005 and 18 November 2005. It is additionally noted that the summary of invention also appears to paste several paragraphs of text from the detailed description in the specification as the summary for the brief.

The remarks filed in the brief again concede that Kimura's circuit adds feedback data to input data, but refuses to accept the Kimura circuit as an accumulator. While Kimura et al. may not use the term accumulator a brief study of Kimura figure 1 reveals that the addition circuit adds feedback data which had been in the feedback path sample delay to the input data and again latches this in the feedback path latch, which meets the definition of accumulation. Kimura also separates the bits by significance (D0-D7 & D8-D15), i.e. low order and high order, and has separate adders for the lower order bits and higher order bits and the accumulation for the respective lower order and higher order bits appears separate as can be seen in the numbering of the lines

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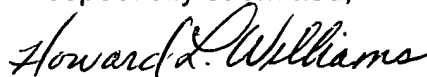
provided between the adders (34, 40; fig. 1) and the latches (36, 46; fig. 1) to indicate the number of result lines. Carry bits from the adders/accumulators are passed up from the lower order chain to the higher order chain (delays 38, 48; fig. 1) and from the higher order accumulators to the output combiners (adders 56, 60, 62; fig. 1). Kimura also discloses plural adders/accumulators connected together for both the high order and low order bits. The first accumulator for the lower order chain of accumulators is provided by adder 34 which receives and adds the eight bits of lower order input data D7-D0 and eight bits of data from delay 36; the sum is passed back to the delay 36 with a carry bit, if generated, passed up to the high order chain. The sum is also fed to the next accumulator stage (adder 45). A similar arrangement is provided for the first accumulator of the high order accumulator chain --adder 40, delay 36 and carry bit to delay 46. The high order accumulator has a delay stage 32 at the input in order to match the timing, i.e. give the low order stage an opportunity to get its result.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,




Howard L. Williams
Primary Examiner
Art Unit 2819

Conferees:



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